INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (SEPARATE SHEET)

International application No.
PCT/EP/2004/052518

Concerning point V.

1. Reference is made to the following document in the present notification:

D1: CHOI M ET AL: "A 6b 1.3G Sample/s A/D converter in 0.35/spl mu/m CMOS" IEEE JOURNAL OF SOLID STATE CIRCUITS, December 2001 (2001-12), pages 1847-1858, XP002316175
D2: US-B1-6 169 510 (BULT KLAAS ET AL) January 2 2001 (2001-01-02)
D3: VORENKAMP PIETER ET AL: "A 12-b, 60-M Samples/s Cascaded Folding and Interpolating ADC", IEEE Journal of Solid-State Circuits, Vol. 32, December 1997.

2. INDEPENDENT CLAIM 1

2.1 The present application does not fulfill the conditions stated in PCT article 33(1), the subject matter of Claim **1** not being in accordance with the inventive step criterion defined by PCT article 33(3).

2.2 D1, which is regarded as the closest state of the art, describes a comparison circuit for an analog/digital converter comprising,

- a network of comparators **(see D1 figures 2, 13 and 15 "comparator" elements)** each comparing an analog voltage to be converted, each comparator comprising a direct output and an inverse output **(see D1 figure 13 "+" and "-" outputs)**, in which each output, direct or inverse, is connected either to inputs of a first network of resistors **(see D1 figure 13 chain of resistors connected to the "+" output)** delivering at its outputs mean voltages that are the average of those present on direct outputs of comparators receiving reference voltages similar in their distribution over the range, or to inputs of a second network of resistors **(see D1 figure 13 chain of resistors connected to the "-" output)** delivering at its outputs mean voltages that are the average of those present on inverse outputs of comparators receiving reference voltages similar in their distribution over the range.

2.3 The subject matter of Claim **1** differs from **D1** in that:

a) each comparator receives an analog voltage to be converted and compares it with a reference voltage, these reference voltages being distributed over a range in which the analog voltage may vary;

b) each direct or inverse output is linked to the input of a voltage follower, the outputs of each voltage follower being connected to the networks of resistors.

2.4 The fact of using reference voltages distributed over a range to serve as comparison with an analog input signal to be converted is well known **(see for example D2 figures 1 and 2)** and constitutes merely the unipolar alternative to the input of each comparator for performing the comparison **(while D1 describes a differential solution)**. The person skilled in the art would choose the appropriate alternative to match the application or the demands/restrictions of the application without exercising any inventive step.

Moreover, this characteristic does not contribute in any manner in respect of the invention, since it constitutes the input of the circuit whereas it is at the output only that the elements necessary for the embodiment of the invention as described in the present patent application are placed.

2.5 The use of voltage followers between the outputs of the comparators and the networks of resistors make it possible not to lose any signal gain. This function is obvious in respect of voltage followers and the person skilled in the art would not hesitate to consider its use in the comparison circuits of **D1** to improve the signal output by the comparators **(see for example D3 figure 8; page 1881 column 2 lines 5-12)**.

2.6 Consequently the subject matter of Claim **1** does not involve any inventive step PCT article 33(3).

3. DEPENDENT CLAIMS 2-4

The claims contain no characteristics which, combined with the characteristics of any claim to which they refer, satisfy the requirements of the PCT as regards inventive step (PCT article 33(3)) since they are considered to be obvious:

* The additional characteristics of Claims **2 and 3** are considered to be details of the invention.

* The subject matter of Claim **4** is already anticipated by document **D3 (figure 8)**.